REMARKS

The specification has been amended to correct typographical and grammatical errors. Also, the specification has been amended to correct references to the IB inbound processor 108 and IB outbound processor 109 such that the specification is consistent with Fig. 1. Finally, Fig. 2 has been corrected to correspond to the patent specification.

Claims 1-17 and 19-20 are active in the application. Claims 19 and 20 have been added and claim 18 has been canceled.

The subject matter of claim 18 has been incorporated into claim 1.

Claim 19 is supported in the specification at page 3, lines 17-20 and page 10, lines 16-18. Frames that are "related" are understood to belong to the same sequence.

Claim 20 is supported by the specification at page 5, lines 11-12, and by Fig. 1.

Claim 1 has been amended to specify that thread units are operable for performing communications protocol conversion. Protocol conversion can be, for example, conversion between Fibre-Channel (FC) protocol and Infiniband protocol (IB), or other protocols such as 10 gigabit Ethernet, or Internet protocol (IP) (see page 2, lines 12-24). Protocol conversion is an essential, fundamental feature of the invention, and is described throughout the present specification. For example, Fig. 1 shows a system for converting between fibre channel (FC) and Infiniband (IB) protocols.

Protocol conversion is the conversion of data into a different format for transmission or processing. For example, in a fibre channel communications protocol, each data frame contains up to about 2 kilobytes of data, in combination with a header containing address information. Other kinds of protocols may have larger or smaller data frames, and headers with different formats. In order for different networks employing different protocols to communicate with one another, a protocol converter is required that changes the size of data frames, and changes the formatting and type of header information.

The present invention provides a system for converting communications data between communications protocols. In the present system, multiple programmable processors are used to perform the conversion. Each of the multiple processors comprises multiple threads, with each thread capable of executing distinct instructions. The

architecture of the present protocol converter is easily programmable and adaptable to accommodate many different kinds of protocols, and accommodate changes to existing protocols. Also, the system is operated such that the processors perform the conversion utilizing parallel and pipelined processing. Parallel processing methodology is described in the present specification at page 11, line 25 through page 12, line 27. Pipelined processing methodology is described in the present specification at page 13, line 1 through page 14 line 6. Because of these features, which are recited in claim 1 as amended, the present invention provides a protocol conversion system that is easily adaptable to meet the demands of new, still-evolving network systems (see page 2, lines 19-24). Also, owing to the parallel and pipelined methodology, the present invention provides a balanced and efficient usage of the multiple processors.

Claims 1-12 and 18 were rejected under 35 USC 103(a) as being unpatentable over US patent 6,393,026 to Irwin in view of US Patent 6,606,704 to Adiletta et al. These rejections are traversed.

Irwin teaches a data packet processing system and method for a router to route data packets in a network. Irwin teaches the use of multiple processors, and specifically, a master processor and slave processors. There are two fundamental differences between the present invention as claimed, and the teachings of Irwin.

Firstly, Irwin does not teach or suggest communications protocol conversion, as required by amended claim 1. The system of Irwin is used only for data packet routing. In Irwin, the master node (processor) receives data packets which are then sent to slave nodes for forwarding (e.g. see col. 3, lines 50-60, col. .6, lines 48-61). Irwin discusses the use of various data protocols such as Internet protocol (e.g. see col. 1, lines 11-22) However, nowhere does Irwin teach that data packets or data frames can be converted between different types of protocols (e.g. between fibre channel protocol and internet protocol, for example). Irwin does not teach or make use of protocol conversion. In Irwin, routing is performed, which is the process of sending data packets to the correct electronic address or server. Routing is fundamentally different from protocol conversion, and in many computer network applications, protocol conversion and packet routing will be used together. However, routing does not include or require protocol conversion.

In reference to canceled claim 18, which requires protocol conversion, the Office Action argues that Irwin teaches protocol conversion in col. 1, lines 13-22. In this section, Irwin does teach connectivity between computer networks via Internet protocol (IP). However, Irwin does not teach or suggest that the networks can have different communications protocols, and does not teach or suggest how to perform such conversion if conversion was needed. Col. 1, lines 13-22 of Irwin teach only that a single protocol, specifically Internet protocol (IP), is used to locate and route data between the networks. Irwin does not teach or suggest protocol conversion in Col. 1, lines 13-22 or anywhere else.

Secondly, Irwin requires the use of a master processor and slave processors. In Irwin, the master processor distributes data packets among slave processors for forwarding. In the present invention, parallel processing is necessarily performed and is required in claim 1 (parallel processing is described in the present specification on page 12). In parallel processing, as employed in the present invention, there is no master processor, and no slave processors. The processors of the present invention operate with the same or similar functionality, without a master-slave functional relationship. However, it is noted that in the present invention one of the processors can have dispatcher functionality, which controls traffic between the other processors. In the present invention, any one or any combination of multiple processors can provide dispatcher functionality. It is well-known that dispatcher functionality is distinct from master-slave functionality.

Adiletta et al. does teach the use of processors containing multiple thread units, and does teach the use of parallel processing. However, like the Irwin reference, Adiletta et al. completely lack any teaching or suggestion of protocol conversion. Accordingly, no conceivable combination of Irwin and Adiletta et al. could produce the present invention as claimed in claim 1, which is a system for performing protocol conversion. Accordingly, the rejection of claim 1 must be withdrawn.

Additionally, it is noted that pipelined processing is not taught or suggested by Irwin or Adiletta et al. Pipelined processing is required by claim 1, and is another feature distinct over the Irwin and Adiletta et al. references. Adiletta et al. actually distinguishes itself from pipelined processing in col. 1, lines 16-19. Similarly, Irwin does not teach or

suggest pipelined processing. Accordingly, no conceivable combination of Irwin and Adiletta et al. could produce a protocol conversion system employing pipelined processing. Hence, the rejection of claim 1 must be withdrawn for this addition reason.

Regarding claim 3, neither Irwin nor Adiletta et al. teach memories with areas for storage of payload and header information, or storage areas for protocol-specific information. Protocol-specific information is not employed in Irwin or Adiletta et al. because they employ only a single protocol, and do not convert between protocols. Hence no memory is required for protocol specific information. Also, neither Irwin nor Adiletta et al. teach or suggest separately storing header and payload data information. Such separate storage of header and payload is not necessary in the prior art references because protocol conversion is not being performed.

Claim 12 has been amended to specify that the hardwired logic front end includes components for transmitting and receiving data in each of two types of protocols. Both transmit and receive functionality with two types of protocols is necessary in the invention because the processors must be able to have 2-way communication with at least two types of protocols. Support for the amendments to claim 12 is explicit in Fig. 1, which shows transmit and receive functionality for both FC and IB protocols.

Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Irwin and Adiletta et al. further in view of US Patent 6,629,257 to Hartwell. This rejection is traversed. While Hartwell teaches the use of Internet Protocol (IP), Hartwell does not teach or suggest protocol conversion. Therefore, Hartwell cannot compensate for the deficiencies of the Irwin and Adiletta et al. references.

Claims 14 and 15 were rejected under 35 USC 103(a) as being unpatentable over Irwn, Adiletta et al., further in view of US Patent 5,513,354 to Dwork et al. This rejection is traversed. Dwork does not teach or suggest protocol conversion, and so Dwork cannot compensate for the deficiencies of the Irwin and Adiletta et al. references.

Claim 16 was rejected under 35 USC 103(a) as being unpatentable over Irwin, Adiletta et al., and Dwork in view of US patent 4,674,034 to Iwashita. Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Irwin, Adiletta et al., and Dwork in view of US patent 5,428,766 to Seaman. These rejections are traversed. Neither Iwashita nor Seaman teach or suggest protocol conversion, and so neither of

these references can compensate for the deficiencies of the Irwin, Adiletta et al., and Dwork references.

Regarding claim 19, neither Irwin nor Adiletta et al., nor any of the other references teach or suggest that related data frames from the same sequence are processed at the same thread unit. Employing a single thread unit to process multiple, related frames tends to reduce processing time.

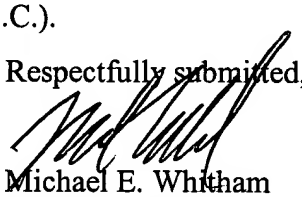
Regarding claim 20, neither Irwin nor Adiletta et al. nor any of the other references teach the use of four processors providing inbound and outbound processing for two protocols in a protocol converter.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1-17 and 19-20 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees for the petition or for entry of this amendment to Attorney's Deposit Account No. 50-2041 (Whitham, Curtis & Christofferson P.C.).

Respectfully submitted,



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Amendments to the Drawings

Concurrently filed herewith are formal drawings for the application.

Attached hereto, in connection with Figure 2 of the application, attached is an annotated sheet of Figure 2 and a replacement sheet of Figure 2. The text of item 207 has been changed to ALU, as is noted on page 6, line 5 of the patent specification as originally filed. Approval and entry of the replacement sheet in the next action is requested.

ANNOTATED SHEET

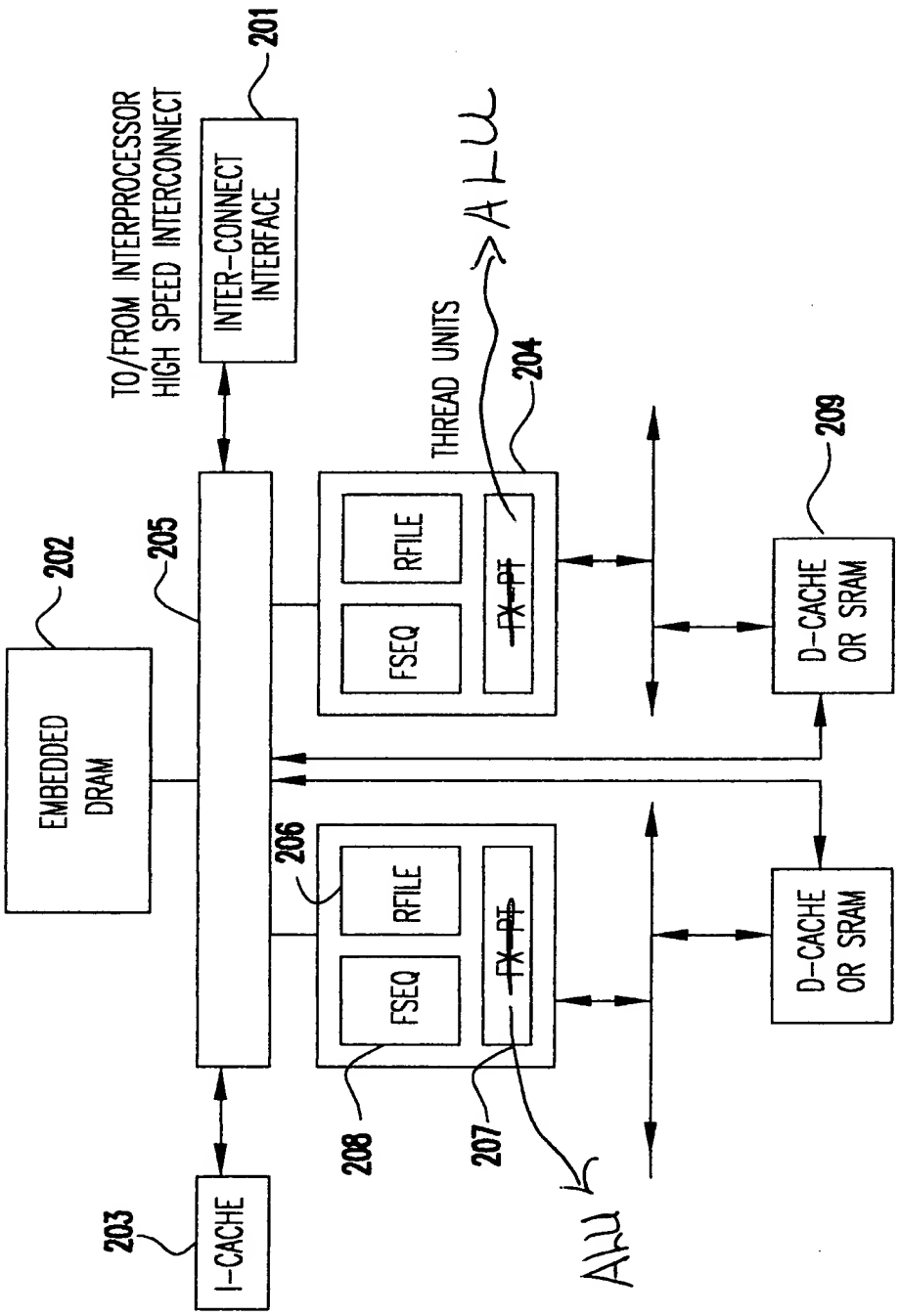

FIG.2